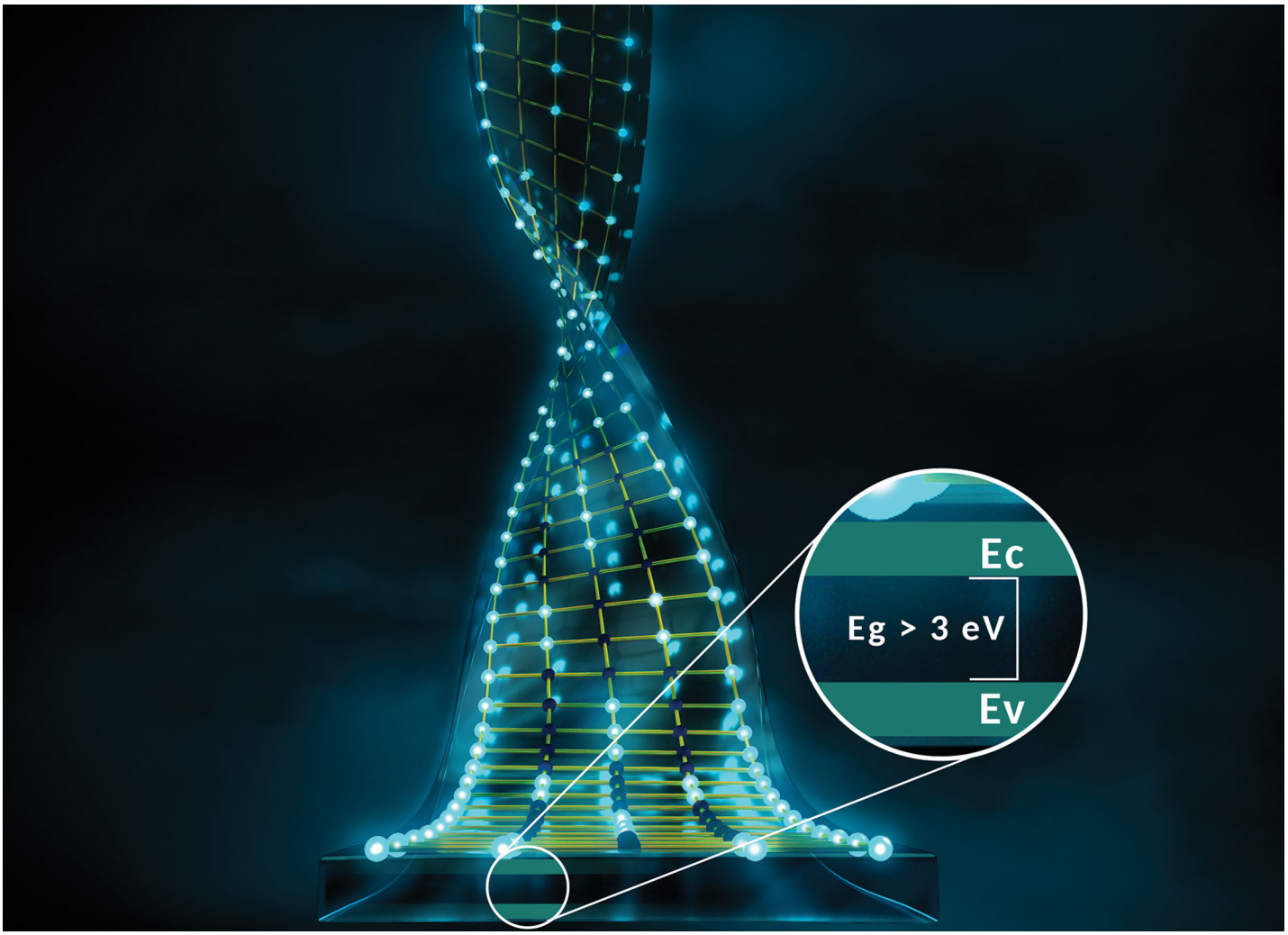

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Recent advances in free-standing single crystalline wide band-gap semiconductors and their applications: GaN, SiC, ZnO, β-Ga_2O_3, and diamond

The recent advances in free-standing wide band-gap membranes, including GaN, SiC, ZnO, β-Ga_2O_3, and diamond and their applications are highlighted. Fabrication techniques and material characterization of each membrane are presented with its device applications.

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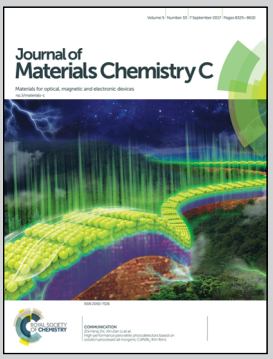

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Recent advances in free-standing single crystalline wide band-gap semiconductors and their applications: GaN, SiC, ZnO, β-Ga_2O_3, and diamond

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Free-standing single crystalline semiconductor membranes have gained intensive attention over the last few years due to their versatile usage in many applications. This material platform possesses a high level of material quality similar to their bulk counterparts because single crystallinity is maintained. Si, Ge, and III–V based membranes have been widely studied for flexible electronic and optoelectronic devices such as thin-film transistors and photodetectors. However, the current status of research and development on free-standing single crystalline wide band-gap membranes is at a relatively early stage compared to IV and III–V based membranes. This review highlights recent advances in free-standing wide band-gap membranes, including GaN, SiC, ZnO, β-Ga_2O_3, and diamond and their applications. Fabrication techniques of each membrane are presented with material characterization. Some prospects for new research opportunities and challenges are also discussed.

1. Introduction

While group IV or III–V based device technologies face several technical issues, such as limited detection wavelength range or low power handling capability, wide band-gap (WBG) semiconductors, which have band-gaps greater than 3 eV, such as GaN, SiC, ZnO, β-Ga_2O_3, and diamond, have gained popularity as a key material for applications in high performance optoelectronic and electronic devices.[1–3] These WBG semiconductors have two definitive advantages for optoelectronic and electronic applications due to their large band-gap energy. WBG energy is suitable to absorb or emit ultraviolet (UV) light in optoelectronic devices. It also provides a higher electric breakdown field which allows electronic devices to possess higher breakdown voltages. WBG based devices can be categorized into light emitting, sensing, and high power devices. Firstly, the representative lighting devices are blue or UV light emitting diodes (LEDs) and lasers.[4,5] While GaN and ZnO are broadly applicable to light emitting applications due to their direct band-gap, other indirect WBG materials such as SiC, Ga_2O_3, and diamond are almost exclusively used for photodetector (PD) applications due to their superior UV sensing capability.[3] Secondly, representative electronic devices are high power diodes and field effect transistors (FETs). These devices can operate at higher voltages with lower leakage currents due to the high critical electric field of the WBG semiconductors compared to Si. In addition, the higher thermal conductivity of SiC allows SiC-based electronic devices to work at higher power densities and higher temperatures than GaN-based electronic devices. However, the formation of two-dimensional electron gas (2DEG) at the AlGaN/GaN interface due to the spontaneous and piezoelectric polarization in the AlGaN barrier layer enables GaN-based electronic devices to operate at a high power and frequency regime.[6]

The abovementioned WBG devices, however, have been mainly fabricated using thin-film or one-dimensional (1D) nanostructures (*e.g.*, nanowires and nanorods)[7–9] in which their starting substrate plays an important role in material quality and performance. In recent years, the development of free-standing single crystalline WBG semiconductor membranes has attracted more attention because they not only offer unique material properties but also enable us to demonstrate unconventional forms of electronic and optoelectronic devices.[10] They are very thin (hundreds of nanometers down to a few atomic layers) and obtain good material uniformity, mechanical flexibility and durability, and electrical properties equivalent to their bulk counterparts. However, unlike the creation methods for Si, Ge or III–V based free-standing single crystalline

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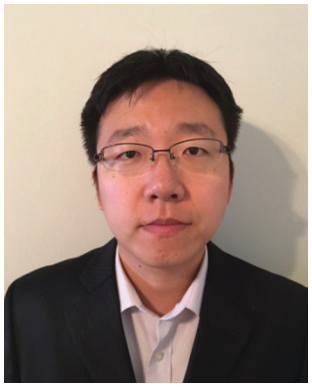
semiconductor membranes,[11–16] most of the WBG semiconductors do not have a good sacrificial layer that allows the WBG semiconductor layer to separate from the bulk substrate, therefore each WBG semiconductor has a unique method to form a free-standing format such as smart-cut, laser-lift off (LLO), aqueous growth, and mechanical exfoliation.

Fig. 1 shows the reported thickness of free-standing WBG semiconductor membranes as a function of band-gap energy



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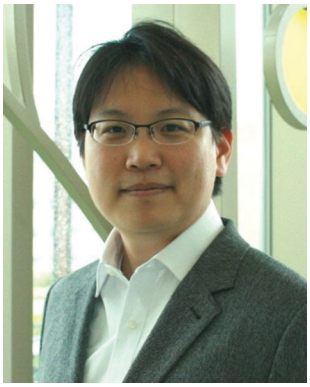

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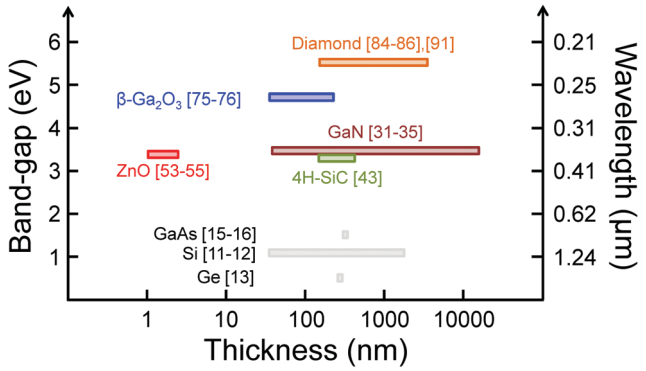

Fig. 1 Band-gap energy (eV), its corresponding wavelength (μm), and thickness (nm) of various semiconductor membranes.

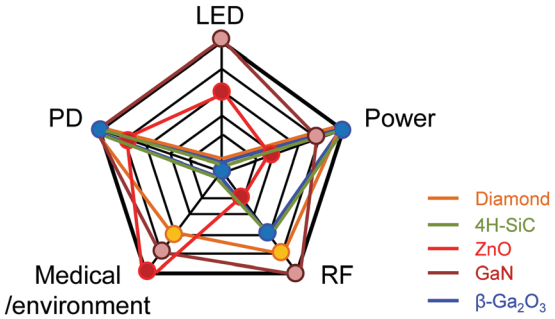

Fig. 2 Application chart of single crystalline free-standing WBG membranes.

and their converted wavelength. All physical parameters shown in Fig. 1 are based on the references cited in this paper. The thickness of each membrane can be easily tuned using physical or chemical thinning methods. Typically, the thicknesses of free-standing WBG semiconductor membranes are a few hundreds of nanometers, but some WBGs such as ZnO can be reduced down to a few atomic thickness. Since flexural rigidity is drastically reduced in this thickness range, high mechanical flexibility is expected, enabling flexible, bendable, and stretchable applications. Such additional mechanical characteristics also open the possibility of altering the physical properties from their bulk materials by inducing strain to crystalline layers. Table 1 summarizes some important material properties of WBG semiconductors that are highlighted in this review.[17–19] The material properties of Si, Ge, and GaAs were included for comparison.

In Fig. 2, the application chart shows the potential or current use of devices based on single crystalline free-standing WBG semiconductors. ZnO has great potential to power, LEDs, and medical applications due to its direct band-gap and good biocompatibility. SiC and β-Ga_2O_3 have potential for PD and power electronics due to their relatively high breakdown electric field and thermal conductivity. GaN has been used in many applications from radio frequency (RF) to PD and LEDs, covering power and medical applications. Lastly, diamond has been successfully used in power, PD, and medical applications, with some effects toward RF applications as well. All of these single crystalline WGB membranes can be an ideal active material for future high-performance electronics and optoelectronics. In addition, it is possible to form multifunctional heterojunction devices by integrating the WBG membranes with either inorganic or organic semiconductors, as reported in IV and III–V membranes.[20,21] Therefore, a WBG membrane can also provide a viable material platform, which may play a key role in enhancing the functionality of WBG semiconductors.

In this paper, we present a comprehensive review on the progress and perspectives of WBG semiconductor membranes and their device applications. The fabrication methods and material characteristics of the free-standing WBG semiconductor membranes have been provided. Some prospects for new research opportunities and challenges are also discussed.

2. Materials and applications

(1) GaN membranes

GaN is one of the widely used WBG semiconductors because of its direct band-gap, existence of various dopants, stable crystal structure, and existence of a native substrate which enable it to be used in various optoelectronic, high-power, and high-frequency devices. Over the past decade, numerous research studies have been reported on state-of-the-art technologies in GaN-based LEDs, PDs, and transistors.[22–24] Among them, free-standing GaN membranes have been a prospective material for flexible and stretchable GaN devices. For example, flexible GaN blue LEDs are essential parts of implantable devices for biomedical applications.[25] GaN membranes, with a typical thickness of less than a few micrometers, play a crucial role in the recent development of the GaN devices. The existence of GaN membranes has been enabled by several fabrication techniques such as laser lift-off (LLO), conductivity-based selective etching, removal of bottom Si substrates, and high-temperature annealing.

The LLO technique is applicable to the creation of relatively thick GaN membranes (several μm). Fabrication of thin GaN

Table 1 Important material properties of WBG semiconductors covered in this review

	Si	Ge	GaAs	GaN	4H-SiC	ZnO	β-Ga_2O_3	Diamond
Band-gap (eV)	1.12	0.66	1.43	3.39	3.23	3.37	4.8–4.9	5.47
Dielectric constant	11.9	16.2	13.1	8.9	10.1	8.66	10	5.7
Electric breakdown field (kV cm^{-1})	300	100	400	3300	3000	3800	8000	10 000
Electron mobility (cm^2 V^{-1} s^{-1})	1500	3900	8500	1000	900	100–200	300	2200
Hole mobility (cm^2 V^{-1} s^{-1})	600	1900	400	200	120	5–50	—	1800
Thermal conductivity (W cm^{-1} K^{-1})	1.5	0.58	0.46	1.3	4.9	0.5	0.136 [100] 0.228 [010]	150
Saturated electron drift velocity ($\times 10^7$ cm s^{-1})	1	0.65	1	2.4	2	2.4	1.3	3

membranes (several hundreds of nm) is limited because they can be mechanically damaged during the process. Fabrication of devices is possible before the LLO, which can simplify subsequent processes such as interconnection. Thin GaN membranes can be made by conductivity-based selective etching of a highly doped GaN layer that is used as a sacrificial layer. Removal of the bottom Si substrates is another method to create GaN membranes. Removal of the bottom Si substrates can be performed either by dry or wet etching. This approach is effective to obtain large sized GaN membranes because large Si wafers are available. However, it is challenging to grow high quality GaN epi-layers on Si substrates. We present details of each technique for the creation of GaN membranes and their device applications.

The LLO technique has been widely exploited to separate GaN films from their growth substrate (*i.e.*, sapphire).[26–29] It uses a pulsed UV laser from the back side of the substrate to induce localized thermal decomposition of the GaN. Due to the band-gap difference between the sapphire substrate ($\sim$8.6 eV) and the GaN layer (3.4 eV), sapphire is transparent to UV wavelengths and is absorbed in the GaN film. Therefore, the absorbed energy selectively heats up the material and nitrogen gas at the interface allows the GaN membrane to separate from the sapphire substrate. A detailed description of the LLO setup and its process can be found elsewhere.[30]

In the early stages, the LLO technique was used to improve the device performance of GaN LEDs compared to those of the devices on the sapphire substrate. Limitations of the device performance are attributed to poor thermal conductivity and high series resistance of the sapphire substrate. For example, the GaN LED structure was separated from sapphire and transferred onto a Cu substrate.[30] Fig. 3(a) shows the process scheme for the fabrication of the LLO undoped GaN. The LED epi-layer consisted of a 1.5 μm thick n-type GaN layer, five periods of 2/5 nm thick InGaN/GaN multi-quantum wells (MQWs), and a 0.3 μm thick p-type GaN layer. The quality of the LLO film was characterized using X-ray diffraction (XRD) and photoluminescence (PL). As shown in Fig. 3(b) and (c), a similar value of the full width at half maximum (FWHM) and a PL spectrum before and after the LLO process confirmed the compatibility of the LLO technique with device fabrication. In this example, the LEDs on Cu were functional up to 400 mA, while the light output power of the regular LEDs on sapphire saturated at $\sim$225 mA (Fig. 3(d)). The high operation current was attributed to the improved heat dissipation capacity of the LLO processed LEDs.

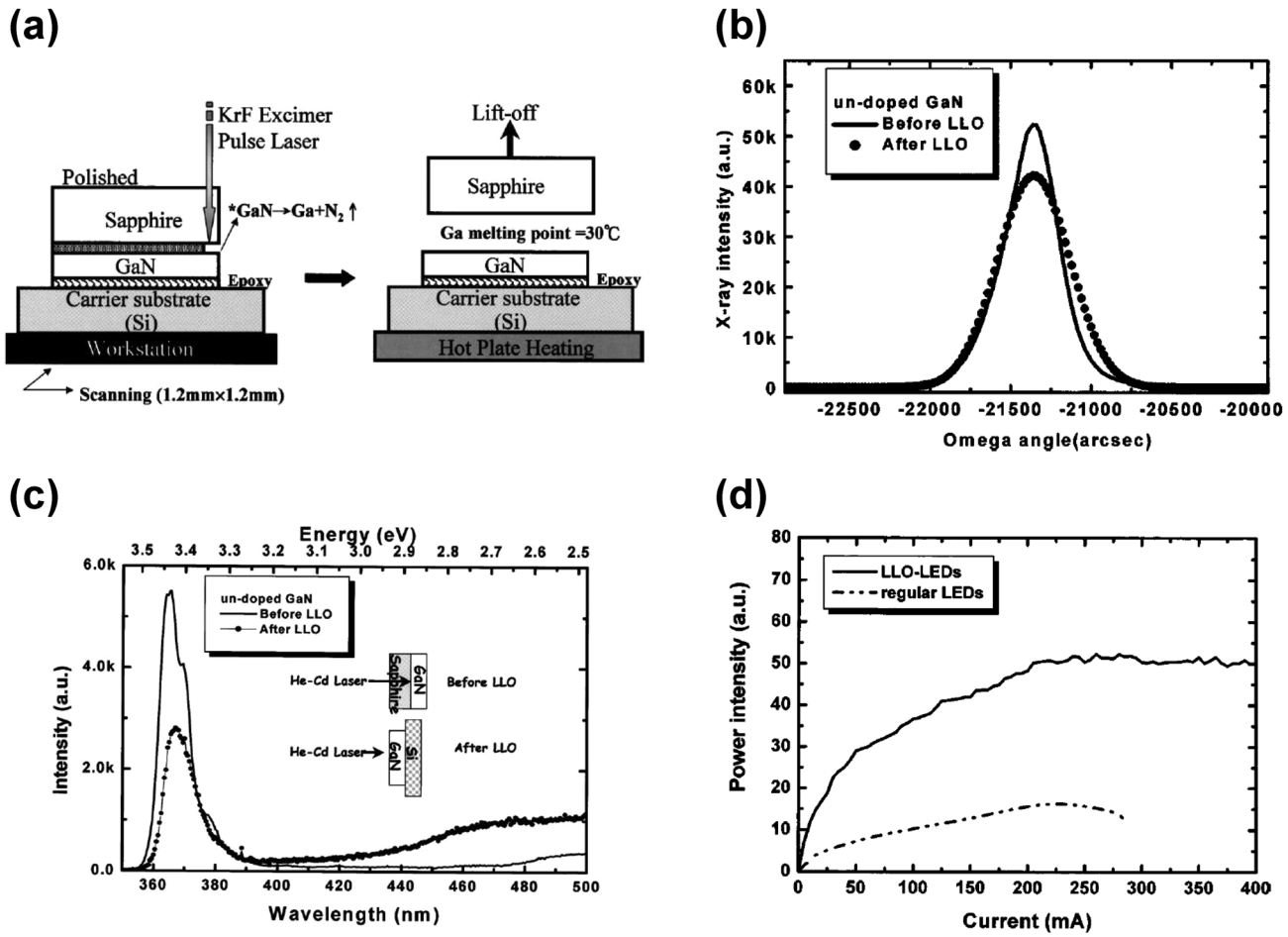

Fig. 3 (a) Process scheme for the fabrication of the LLO undoped GaN. (b and c) XRD and PL spectrum of the undoped GaN before and after LLO. (d) Light output power–current (*L*–*C*) characteristics for the LLO-LEDs on Cu, and the regular LEDs on sapphire under high current cw operation conditions. Reproduced with permission from ref. 30. Copyright 2004, American Institute of Physics.

In recent years, the LLO technique has become a viable method to fabricate flexible LEDs for a variety of applications from deformable displays to wireless optogenetics.[31,32] LLO is combined with different techniques to realize flexible LEDs. Typically, GaN LEDs are initially fabricated on epitaxial GaN on sapphire. The LLO process is the same, but the subsequent removal process slightly differs. Fig. 4(a)–(d) show schematic illustrations and images corresponding to steps for creating transferable GaN LEDs grown epitaxially on sapphire substrates. Eutectic bonding is used to support the sapphire on Si handling substrates.[33] A thin layer (200 nm) of SiN_x is deposited on the fabricated GaN LEDs, followed by the deposition of Cr/Pd/In (15/150/900 nm). The devices are flipped and bonded with Si by eutectic bonding. The bottom sapphire substrate faces up and UV light is exposed to remove the Ssapphire. An agglomerated $InPd_x$ layer tethers the LEDs to the underlying Si substrate. Undercutting the $InPd_x$ and Cr releases the LEDs, which are picked by patterned PDMS. The LEDs are removed from the patterned polydimethylsiloxane (PDMS) and transferred on either polyethylene terephthalate (PET) or glass. The electrical and optical properties of LEDs on sapphire and PET are nearly identical. Arrays of LEDs on a strip of PET show a high level of deformability as shown in Fig. 4(e).

The thickness of the GaN layers released using the LLO technique is a few micrometers (μm). Recently, another class of GaN membranes, which have thicknesses less than a few hundreds of nanometers (nm), has been reported.[34,35] Release of ultrathin GaN membranes can motivate experimental and theoretical studies on flexible, bendable, and stretchable GaN devices because flexural rigidity can be minimized. A heavily doped n-type GaN with a doping concentration larger than 1×10^{18} cm^{-3} can be selectively removed by electrochemical etching with oxalic acid. This enables the heavily doped GaN to be used as the sacrificial layer for releasing the lattice-matched GaN epilayer from the source wafer. Large area (5×5 mm^2) free-standing GaN membranes as thin as 90 nm can be obtained using hydrofluoric acid (HF) based doping selective electrochemical etching. Fig. 5(a)–(d) show optical, SEM, TEM, and AFM images of the GaN membrane, respectively. A photoresist (PR) served as an elastic mechanical support to ensure the large area transfer. XRD, TEM, and PL confirmed crystalline perfection and optoelectronic efficacy of the released GaN membrane.

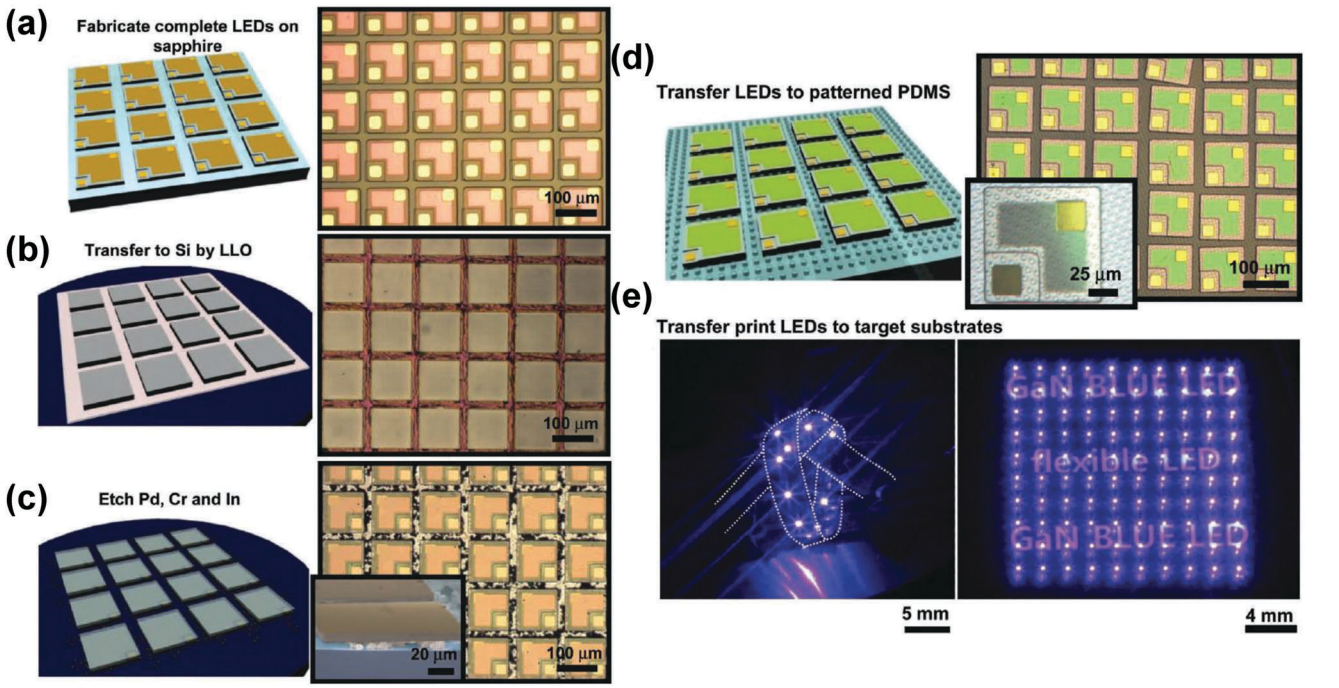

Fig. 4 Schematic illustrations and images corresponding to steps for forming, integrating, and interconnecting ultrathin (~6 μm), microscale inorganic light-emitting diodes (μ-ILEDs) derived from GaN materials grown epitaxially on sapphire substrates. (a) Arrays of μ-ILEDs (100 μm × 100 μm separated by 20 μm; left: schematic; right: optical microscopy image) are first defined, completely, on the sapphire substrate, including L-shaped current-spreading p-contacts (Ni: 15 nm/Au: 15 nm) and square (25 μm × 25 μm) n- and p-contact pads (Cr: 15 nm/Au: 300 nm). (b) Bonding to a silicon wafer using an In–Pd alloy, followed by laser lift-off and removal of the sapphire substrate yields arrays of μ-ILEDs on Si (dark blue). The top sides of the devices (left: schematic; right: optical microscopy image), coated with Ga (gray) from the LLO process, can be cleaned by etching with HCl. This etchant also removes unalloyed In, to leave only In–Pd alloy. (c) Schematic illustration (left), optical microscopy image (right) and colorized, tilted view scanning electron microscopy (SEM) image (right inset) after these etching processes. Only isolated agglomerates of In–Pd (black dots in the optical microscopy image and schematic; pink structures in the SEM) remain. (d) Arrays of μ-ILEDs after transfer to the structured surface of a slab of PDMS (arrays of pillar diameters, heights and spacings of 3, 1.4, and 5 μm, respectively) and complete removal of the residual metal by etchants for Cr and Pd (left: schematic; right: optical microscopy image). A layer of SiN_x protects the μ-ILED metallization from these etchants. The inset on the right shows an individual device. (e) Arrays of μ-ILEDs (12 devices) on a 4 mm × 15 mm strip of PET, tied into a knot to illustrate its deformability (left) and on glass (100 devices; right). Reproduced with permission from ref. 33. Copyright 2012, Wiley-VCH.

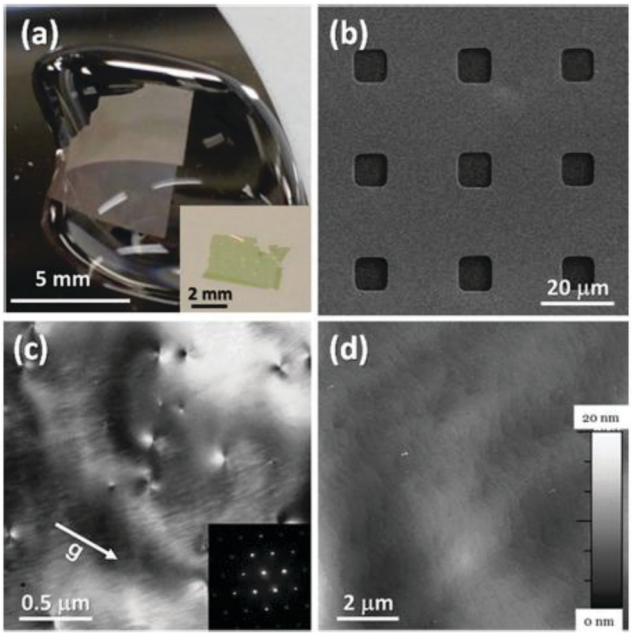

Fig. 5 (a) Separation and unrolling of a large-area GaN membrane on an Si substrate with DI water. Inset shows demonstration of a 300 nm-thick InGaN based membrane structure transferred onto a PET film. (b) Plan-view SEM image of the GaN membrane after being transferred onto the Si substrate. (c) Plan-view TEM image showing dislocations with a density comparable to the as-grown GaN layers. Inset shows selective area electron diffraction along the [0001] axis showing the single crystallinity of the GaN membrane. (d) AFM image of the GaN membrane after transfer onto the SiO_2/Si substrate. Reproduced with permission from ref. 34. Copyright 2014, American Chemical Society.

Various GaN devices such as LEDs and FETs were fabricated on the released GaN membranes. Although the devices achieved good performance, the flexibility and reliability of the devices were not reported.

While the above approaches separate GaN layers from the sapphire substrate, there exists another method to create GaN membranes from GaN on Si substrates. GaN device structures on Si substrates are grown using metal organic chemical vapor deposition (MOCVD). Removal of the original Si substrate is carried out using SF_6 and SF_6/O_2 plasma etching. Partial removal of Si under the GaN device layers is also demonstrated by wet etching to release and transfer the GaN films.[36] GaN epitaxy on the Si substrate is very attractive and promising because large Si wafers up to 12 inch are commercially available at a low cost. However, the lattice mismatch between Si and GaN (17%) causes a high dislocation density in the GaN layer. In addition, cracks can be generated by the thermal expansion mismatch (54%) if the stress is not controlled within the fracture toughness of GaN. Therefore, the above issues should be overcome to achieve the epitaxial growth of high crystalline crack-free GaN on Si substrates. Although new techniques such as insertion of multiple low-temperature AlN interlayers, selective area growth, and growth on porous Si were proposed, the crystalline quality of GaN on Si was still poor compared to that of the GaN grown on sapphire.[37] Deposition of the sub-monolayer *in situ* SiN_x followed by coalescence growth was developed to enhance the crystalline quality.[38] However, it generates tensile stress during the coalescence growth attributed to the compressive stress of the underlying GaN layer.

Successful growth of GaN LED epitaxial structures on 8-inch Si(111) substrates was demonstrated.[39] The optimized transition layer consists of a stress compensation layer and dislocation reduction layer. GaN LED layers (*i.e.*, p-GaN, InGaN/GaN MQW, and n-GaN) were grown on top of the transition layer. High crystalline quality was confirmed by the highly uniform distribution of the measured PL peak wavelengths of the InGaN/GaN LEDs and FWHM values of the ω-rocking curves of the n-GaN templates across the 8-inch Si substrate. Fig. 6(a)–(d) show measured XRD FWHM values of the n-GaN template and PL peak wavelength of InGaN/GaN LEDs on an 8-inch Si substrate. The measured standard deviation of the dominant wavelength (438 nm) was as small as 2.25 nm. The FWHM values of GaN (0002) and GaN (10–12) were measured to be 220 and 320 arcsec, respectively. In addition, high-efficiency blue LEDs (size: 1.4 × 1.4 mm^2) showed an overall output power and a driving current of 480 mW and 350 mA, respectively, at 3.2 V, which are similar to those of same size LEDs on sapphire. Although an experiment on bottom Si substrate removal was not performed in this work, this demonstration shows that GaN on Si can be an attractive starting material to realize GaN membranes with device quality.

The GaN membrane can be released from the original Si substrate by a partial undercut wet etching of Si.[36] This technique exploits large different etching rates along the (110) and (111) planes of the Si. The wet etching along the plane of Si(110) is about 100 times faster than that of Si(111) with wet chemical etching of potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). Fig. 7(a) shows a schematic overview of the fabrication process. A InGaN/GaN LED membrane (total thickness: 4.8 μm) on a Si(111) wafer is the starting material. The device arrays are arranged such that two sides of the device lie perpendicular to ⟨110⟩. The devices are fabricated by standard processes such as ICP-RIE etching, metal deposition, and subsequent metal annealing for ohmic contacts. Anisotropic undercut etching of the Si was performed by KOH immersion at 100 °C. Break-away anchors prevent the devices from floating during undercut and also served as fracture points during the transfer process. Transfer printing of the devices from the source wafer to a target substrate is performed by a PDMS stamp. The devices are transferred on plastic or glass substrates to form arrays. For the metal interconnection process, *via* are formed by back-side exposure (BSE) on a photosensitive polymer (BCB). The final interconnect metal (Ti/Al) is sputtered and patterned by photolithography and metal etching. Optical images of various lighting modules are shown in Fig. 7(b) and (c). The measured current density–voltage (*J*–*V*) and emission spectrum before and after transfer show almost identical characteristics. In addition, the reliability of the device is tested by measuring the forward voltage at 10 mA of current from the bent devices at various bending radii and bending cycles. No degradation is observed up to 1000 bending cycles.

A new type of GaN membrane enables electrochemical energy storage applications such as supercapacitors with a stable

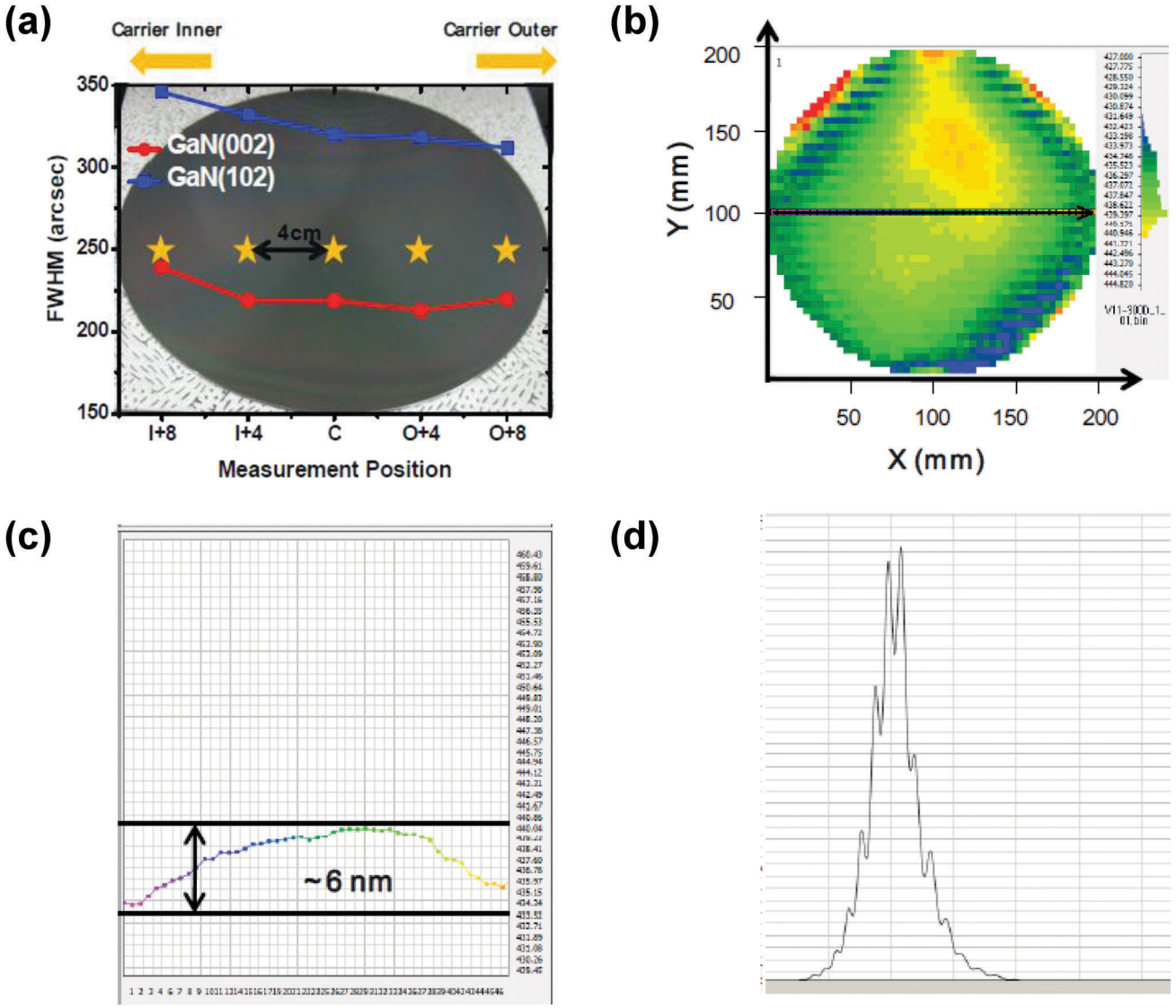

Fig. 6 (a) XRD FWHM values of the n-GaN template on an 8-inch Si substrate measured every 4 cm on the basis of the wafer center. Measured PL peak wavelength of InGaN/GaN LED on the 8-inch Si substrate. (b) Dominant peak wavelength mapping. (c) Line profiles along the parallel direction as shown in (b). (d) A typical spectrum. In this case, the standard deviation of the wavelength is 2.25 nm. Reproduced with permission from ref. 39. Copyright 2012, Society of Photographic Instrumentation Engineers.

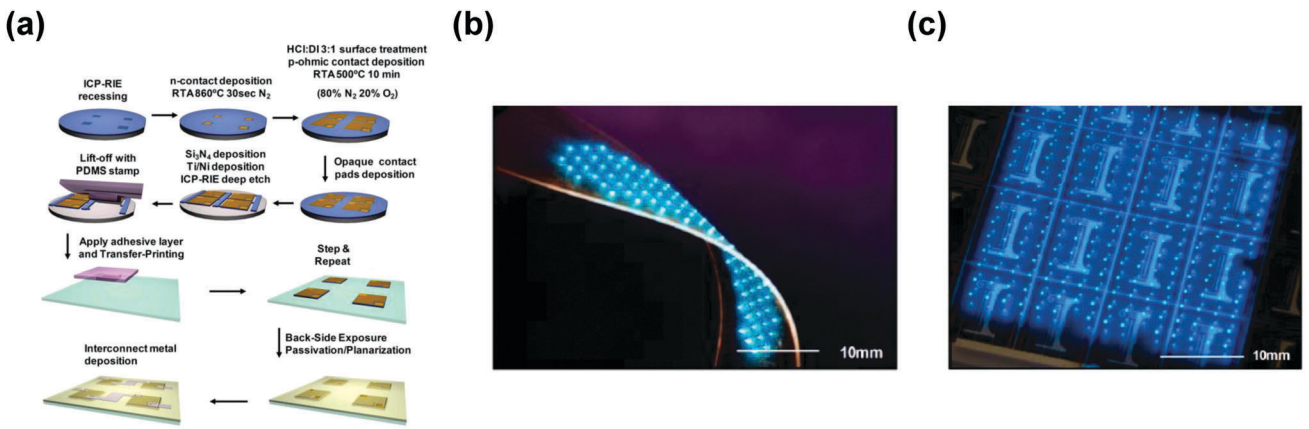

Fig. 7 (a) Schematic overview of the fabrication process. (b and c) Optical images of various lighting modules based on arrays of μ-ILEDs on plastic and glass substrates. Reproduced with permission from ref. 36. Copyright 2011, Proceeding of the National Academy of Sciences.

cycling life, high rate capability, and ultrahigh power density. Single crystalline porous GaN membranes were fabricated using a one-step high-temperature annealing technique.[40] A 5 μm thick GaN layer was grown on a sapphire substrate using MOCVD. V-shaped pits were formed at the dislocation sites in the initial stage of annealing at 1200 °C. As the annealing time increased, the V-shaped pits were enlarged and many voids were formed at the bottom. Finally, the porous GaN membrane was separated from the sapphire after annealing for 80 minutes. The porosity and diameter of the GaN membrane were approximately 70% and 500–800 nm, respectively. Fig. 8 shows a schematic illustration of the fabrication process, surface, and cross-sectional SEM images of the porous GaN membrane. The structural and optical properties of the porous GaN membrane were characterized using XRD, PL, TEM, and Raman spectroscopy. The results confirmed the high crystal quality of the material. In addition, electrochemical characterization of the porous GaN membrane was performed on the fabricated supercapacitors. It maintained 99% of capacitance retention after 10 000 cycles. It also achieved 45 mW cm^{-2} of ultrahigh power density.

(2) SiC membranes

SiC has been known to be the most matured WBG semiconductor since the release of commercial SiC bulk substrates in the early 1990s. Although more than 200 polytypes of SiC have been discovered, two polytypes (*e.g.*, 6H and 4H-SiC) are popular in SiC applications. Its wide band-gap energy (3.03 eV for 6H-SiC and 3.26 eV for 4H-SiC) makes it an ideal material for high power electronic and UV optoelectronic devices.[41] SiC has a higher thermal conductivity (4.9 W cm^{-1} K^{-1}), which is 4 times larger than that (1.3 W cm^{-1} K^{-1}) of GaN. This property enables SiC to be the dominant material for device applications in high-power and high-temperature operation. In addition, SiC has its own stable native oxide (SiO_2) for the application of metal oxide

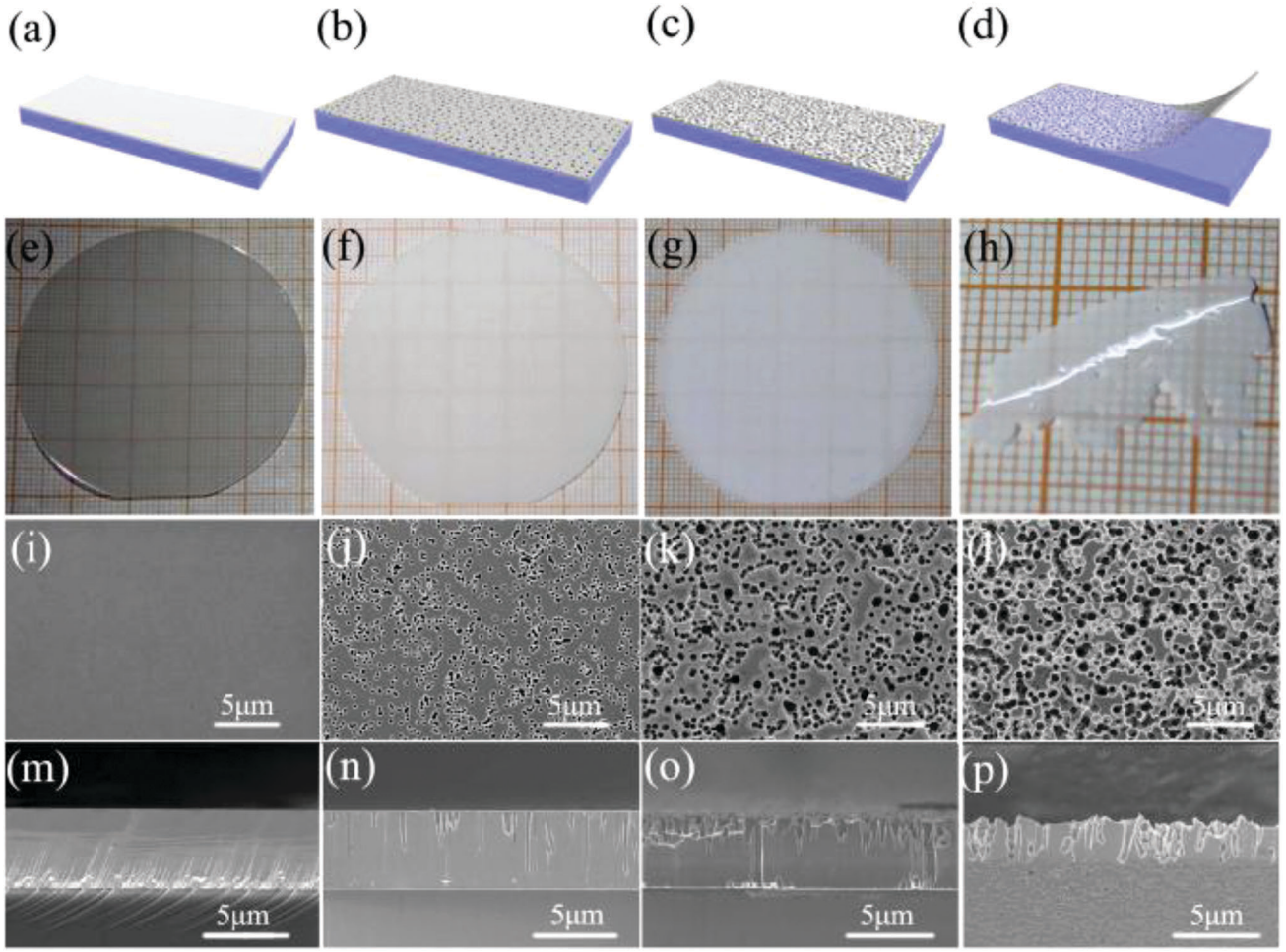

Fig. 8 (a, e, i and m) Smooth surface of as-grown GaN and no pores on the surface and cross section. (b, f, j and n) As annealing time increases (1200 °C, 30 min), many pores appear, and a porous structure is formed. The mean diameter of the pores is approximately 200 nm. (c, g, k and o) After annealing for 60 min at 1200 °C, the size of the pores increased to 500 nm, and many voids have formed at the bottom of the GaN layer. (d, h, l and p) When the sintering time increased to 80 min at 1200 °C, large area and self-separation porous GaN membranes are formed. The pores are distributed evenly over the GaN membrane. The porosity of the porous GaN membrane is approximately 70% (porosity = pore density × single pore area/unit area × 100%). The diameter of the pores is approximately 500–800 nm. The thickness of the porous GaN membrane is uniform at ~3 μm. Reproduced with permission from ref. 40. Copyright 2017, Nature.

semiconductor (MOS) devices. Advanced technology to fabricate SiC epitaxial wafers makes it possible to form a homoepitaxial SiC layer on the SiC substrate. This results in a good crystallographic match between the epilayer and substrate. Despite the competitive advantages of SiC mentioned above, the development of SiC membranes has not been intensively pursued, mainly due to the difficulties in releasing the SiC membrane from the bulk substrate. Therefore, it remains a new area in need of research.

Selective etching of the sacrificial layer is the most common approach to create releasable semiconductor membranes. For example, Si and Ge membranes are obtained from Si on insulator (SOI) and Ge on insulator (GeOI) wafers, respectively.[11–13] These wafers consist of top semiconductor layers, intermediate oxide layers, and bottom handling substrates. The process starts from selectively removing the sacrificial layer (*i.e.*, thermally grown SiO_2) underneath the Si and Ge template layers using hydrofluoric acid (HF). The released membranes are then picked and transferred to a target substrate. Smart-Cut® based on hydrogen (H) ion implantation and wafer bonding is the most practical method to fabricate the SOI and GeOI substrates. Such methods can be utilized to fabricate SiC on insulator (SiCOI) substrates.[42]

Recently, 4H-SiC membranes were developed for potential applications toward high temperature flexible UV PDs.[43] 200 nm thick 4H-SiC membranes were transferred on a PET substrate. The SiC membrane was obtained from the SiCOI fabricated using the Smart-Cut® technique. Partial etching of the underlying sacrificial layer released the SiC membrane, which was subsequently transferred onto PET by a PDMS stamp. Fig. 9 shows optical and microscopic images of the SiC membrane before and after transfer. Similarly good crystallinity (FWHM of XRD rocking curve: 120 arcsec) and surface morphology (RMS surface roughness: 2.39 nm) of the SiC membrane compared to those (30 arcsec and <1 nm) of bulk SiC were confirmed using XRD and atomic force microscopy (AFM). In addition, the optical characteristics of the SiC membrane were comprehensively analyzed in the wavelength range of 200 to 500 nm. The maximum absorption of the SiC membrane was 73.8% at 256 nm with the overall absorption larger than 40% in the wavelength range of 200–260 nm. Furthermore, the reliable flexibility of the SiC membrane was tested on bending fixtures. The absorption spectra remained the same after bending. No cracks or wrinkles were observed from the bent SiC membrane. This SiC membrane is suitable for flexible UV PDs, especially for higher temperature operations. In addition, 4H-SiC membranes can be ideal materials for other applications such as an encapsulating layer for bioresorbable electronics[44] because they are chemically inert and pin hole free.

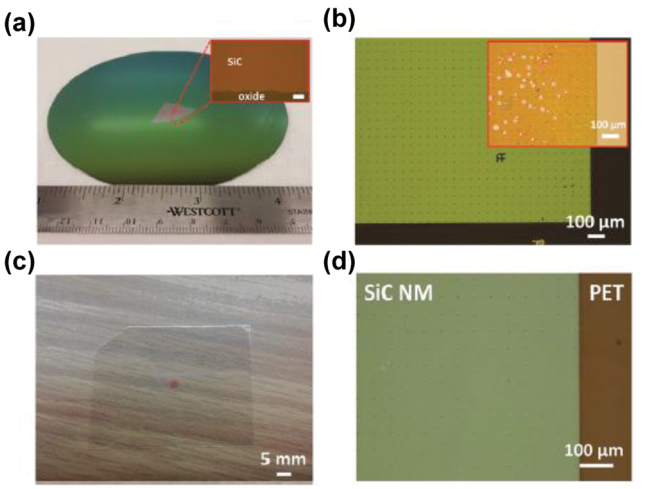

Fig. 9 (a) An optical image of the fabricated SiCOI wafer. The inset shows a zoomed-in microscopy image of the SiC layer of the SiCOI wafer. The scale bar is 200 μm. (b) A microscopy image of the SiC layer of the SiCOI wafer before the undercut process. The inset shows the image after the undercut process is completed. (c) An optical image of the transferred SiC membrane onto a PET film. (d) A zoomed-in microscopy image of the transferred SiC membrane onto the PET film. Reproduced with permission from ref. 43. Copyright 2017, Royal Society of Chemistry.

(3) ZnO membranes

The synthesis of single crystalline ZnO has been well developed by using chemical vapor deposition (CVD), molecular beam epitaxy (MBE), and MOCVD.[45–47] However, the creation of free-standing single crystalline ZnO has several technical issues such as the absence of a sacrificial layer that is lattice matched and etching selective.[48] As an alternative method, free-standing nanowires, nanorods, and nanobelts were demonstrated by vertical growth, followed by separation by pressing, milling, or selective picking.[49–52] However, these approaches only offer nano-meter scale and randomly ordered ZnO nanostructures.

F. Wang *et al.* took a different route by utilizing surfactants (*i.e.*, the close-packed monolayer [Langmuir–Blodgett (LB) films]) to guide the formation of single crystalline ZnO directly at the water–air interface as shown in Fig. 10(a).[53] Submillimeter-sized and a few hundred nanometer-thick single crystalline zinc hydroxy dodecylsulfate (ZHDS) was formed, followed by low-temperature thermal treatment to convert it to a ZnO film (as shown in the microscopic and SEM images in Fig. 10(b)). This approach circumvented the need for single-crystalline substrates to make large-area NMs from materials that do not possess a laminate structure. This surfactant-based single crystalline ZnO synthesis was further refined by introducing an anionic sulfate monolayer, which allows us to precisely control the growth of single crystalline ZnO in a layer by layer fashion as shown in Fig. 10(c).[54] As a result, $\sim$1–2 nm thick single crystalline ZnO nanosheets were successfully synthesized (Fig. 10(d)).

Another approach to create single crystalline ZnO nanosheets used by H.-K. Hong *et al.* is to grow an atomically thin ZnO layer directly on top of a UV/ozone treated graphene layer using atomic layer deposition (ALD) as shown in Fig. 10(e) and (g).[55] Although free-standing ZnO was not demonstrated, this method can offer thin free-standing single crystalline ZnO layers, considering that the graphene layer itself can be free-standing.

In recent years, free-standing ZnO membranes have been applied to various electronic devices that the non-free-standing format of ZnO cannot offer. The energy harvesters and power generators using piezoelectricity of free-standing ZnO membranes

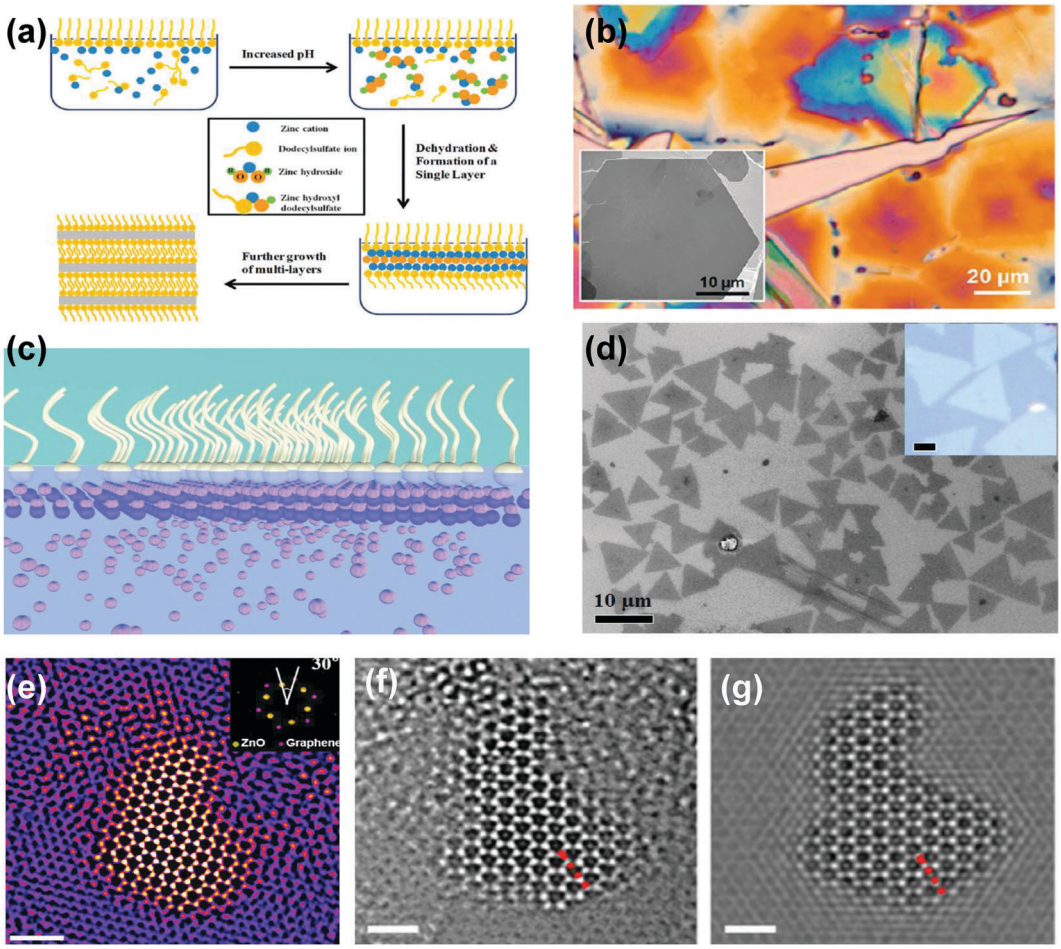

Fig. 10 (a) Schematic illustration of the formation process of ZHDS membranes at the water surface. (b) Microscopy image of a ZHDS membrane. The inset is the hexagonal single crystalline ZnO after the thermal process. (c) Schematic illustration of the formation of ZnO nanosheets directed by surfactant monolayers. (d) SEM image of the nanosheets on a silicon substrate. (e) Atomic resolution TEM image of ZnO misoriented by 30° on graphene. The inset in the upper right corner shows the Fourier transform of the image. (f) and (g) are raw images of Fig. 1(e). Scale bar is 1 nm. Reproduced with permission from ref. 52–54. Copyright 2012, 2016, and 2017, American Chemical Society and Nature.

produce a milliwatt level of output power.[56] Combined with high-performance capacitors or batteries, the energy harvesters or power generators will perform in a practical regime. Another unique application is flexible ZnO FETs. As shown in Fig. 11, various FETs on SiO_2 substrates and plastic substrates were successfully demonstrated.[53,54] However, their relatively low drain current that is associated with difficulties in selective doping or non-existence of p-type ZnO are issues to overcome in order to progress toward high-performance ZnO CMOS applications. Nevertheless, unlike other flexible FETs, ZnO based FETs can offer unique properties such as good bio-compatibility and high transparency on top of decent electrical performance.

(4) β-Ga_2O_3 membranes

Ga_2O_3 is an emerging ultra WGB semiconductor that has seen a lot of activity in recent years for power device and UV detector applications.[57,58] The β-phase of Ga_2O_3 (β-Ga_2O_3) is the thermodynamically stable phase with a large band-gap ($E_g \sim 4.5$–4.9 eV) and large electron mobility making it an attractive semiconductor for next generation power electronics. β-Ga_2O_3 has a base centered monoclinic crystal structure which has implications on transport studies[59] and thin film growth rates.[60] Based on the measured band-gap of Ga_2O_3, a high critical electric field (E_c) is estimated from the empirical dependence of the critical electric field on the band-gap. The large critical electrical field along with large electron mobility gives higher Baliga's Figure of Merit (BFoM) for power device applications. The estimated BFoM is more than that of SiC and GaN which is promising for beyond SiC and GaN power devices.[57,58] While diamond has a higher BFoM than Ga_2O_3, Ga_2O_3 has the advantage of highly matured bulk and thin film growth technology which makes it competitive in terms of cost. Large area doped and semi-insulating bulk crystals of Ga_2O_3 can be grown using scalable crystal growth technologies.[61–65] In addition, both homo- and hetero-epitaxial growth of Ga_2O_3 thin films with excellent doping control have been demonstrated by several growth technologies including MBE,[66–69] halide vapor phase epitaxy[70] and low pressure chemical vapor deposition.[71] These growth technologies have enabled high breakdown Schottky diodes[72] and metal-oxide semiconductor field effect transistors (MOSFETs).[73,74] MOSFET breakdown

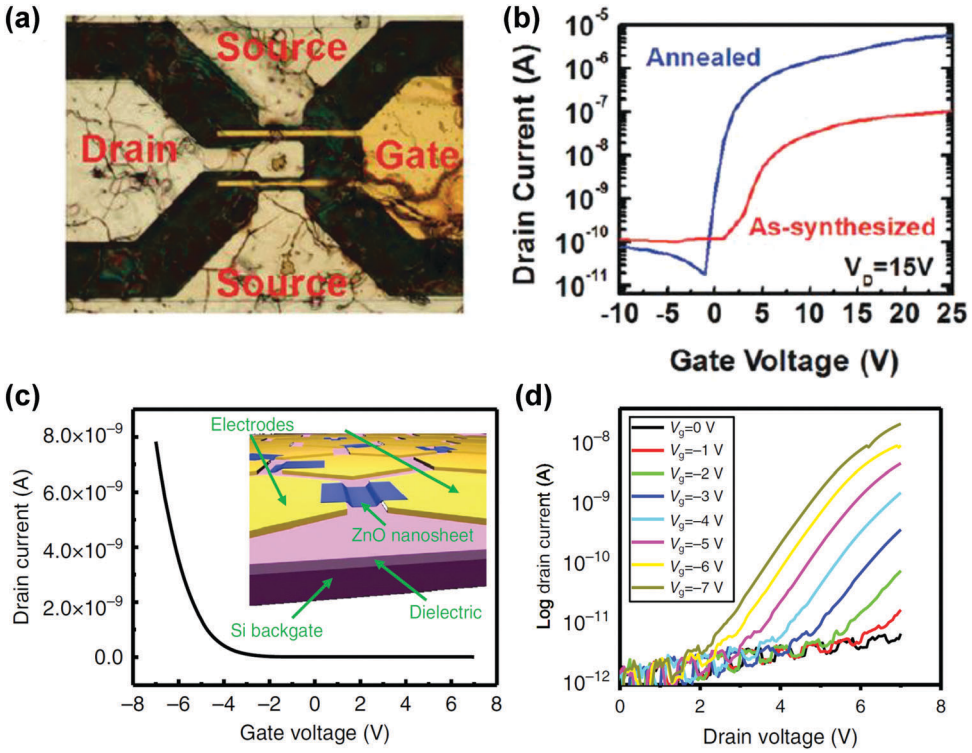

Fig. 11 (a) Microscope image showing ZHDS membrane-based FETs on a PET substrate. (b) Transfer characteristics of FETs before (red) and after (blue) annealing at 95 °C for 48 h. (c) Drain current *versus* gate voltage when the gate voltage scan was from 7 to −7 V with 5 V gate bias. (d) Drain current *versus* drain voltage at different gate voltages from 2 to −7 V with a 1 V step. Reproduced with permission from ref. 52 and 53. Copyright 2012 and 2016, American Chemical Society and Nature.

voltages of 750 V,[73] Schottky diode breakdown voltages of 1 kV,[72] and critical breakdown fields of 3.8 MV cm^{-1} [74] have been experimentally reported, proving the potential of Ga_2O_3 devices.

The choice of dielectrics for the gate barrier and passivation layer has a great influence on the power device performance. Al_2O_3 and HfO_2 have been used as gate dielectrics in Ga_2O_3 devices.[73,75] SiO_2 is an attractive gate barrier material for Ga_2O_3 due to its large band-gap of ~9 eV[76] which can provide higher conduction band offsets to reduce gate leakage. The band alignment between ALD deposited SiO_2 and β-Ga_2O_3 ($\bar{2}01$) is measured using X-ray photoelectron spectroscopy.[77] The measured conduction band offset is 3.6 eV, with the XPS measured band-gap of 8.6 eV and 4.54 eV for ALD SiO_2 and Ga_2O_3 respectively. The calculated band diagram based on the XPS measurements is shown in Fig. 12(a). The conduction band offset calculated from the forward bias Fowler-Nordhiem tunneling current is 3.7 eV, further confirming the XPS measurement. The interface state density between ALD deposited SiO_2 and Ga_2O_3 was calculated using the conductance method and Terman method.[78] The calculated D_{it} (~1 × 10^{12} cm^{-2} eV^{-1}) is shown in Fig. 12(b).

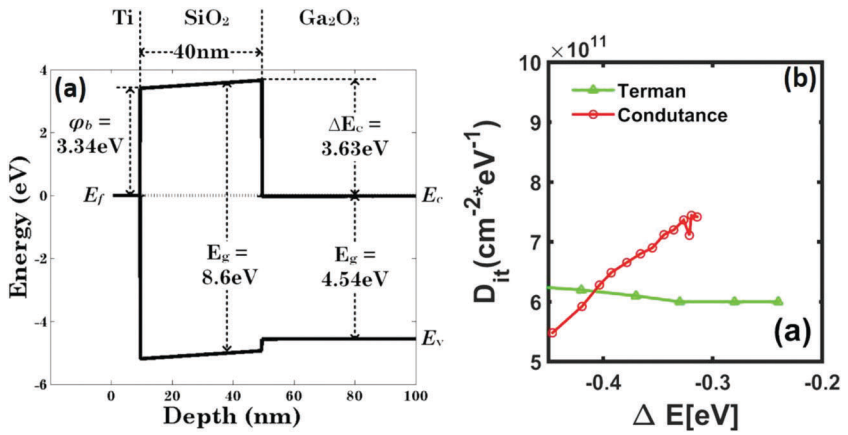

Fig. 12 (a) Calculated band diagram of SiO_2/Ga_2O_3 MOSCAP. (b) Calculated interface state densities (D_{it}) at the SiO_2/Ga_2O_3 interface. Reproduced with permission from ref. 76 and 77. Copyright 2015 and 2016, American Institute of Physics and IEEE.

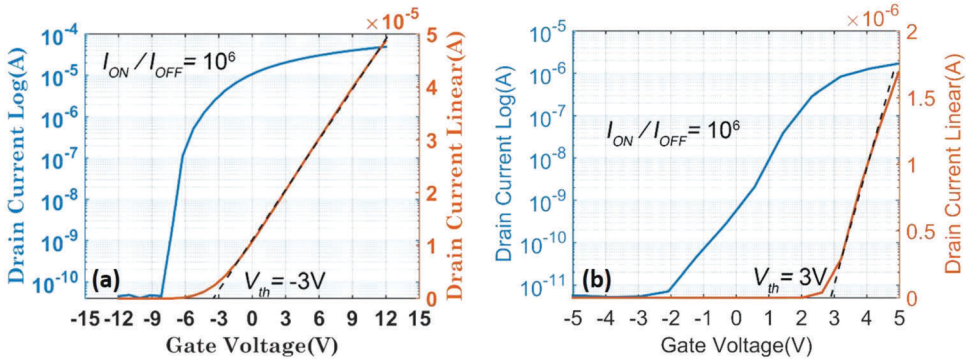

Fig. 13 I_d–V_{gs} characteristics of Ga_2O_3 MOSFETs with ALD SiO_2 as the gate dielectric with (a) Ti/Au gate metal and (b) Pt/Au gate metal. Reproduced with permission from ref. 78. Copyright 2016, IEEE.

The large conduction band offset and low D_{it} make ALD deposited SiO_2 an excellent choice as a gate dielectric for Ga_2O_3 devices.

MOSFETs with ALD deposited gate dielectrics are fabricated on 200 nm MBE grown Ga_2O_3 on semi-insulating Ga_2O_3 substrates.[79] Fig. 13 shows the I_d–V_g characteristics of the MOSFETs with Ti/Au and Pt/Au gates, which show depletion mode operation for Ti/Au and enhancement-mode operation for Pt/Au gates. Both devices show a large ON/OFF ratio of 10^6. The three-terminal breakdown voltage of the devices was ~400 V. The breakdown is a destructive breakdown with a large increase in gate current beyond breakdown. Although these devices show large ON/OFF ratios and breakdown voltages, the drain current densities (I_d ~ 0.1 mA mm^{-1}) are limited by large source contact and access resistances. Incorporation of source/drain doping schemes reduces the parasitic source resistance and increases the drain current with minimal impact on the breakdown voltages.[80]

Experimentally demonstrated device data show the promise of Ga_2O_3 for power devices. However, one major challenge is the low thermal conductivity of Ga_2O_3. Thermal management of Ga_2O_3 power devices is necessary for high power applications. Transfer of the fabricated devices to high thermal conductivity substrates is one potential solution. The base centered monoclinic crystal structure enables the formation of Ga_2O_3 crystalline membranes. The lattice parameters for the monoclinic crystal are a = 12.23 Å, b = 3.04 Å, c = 5.8 Å and β = 103.7°.[60] The easy cleavage plane for the structures is (100) which is along the longest lattice constant. The crystal has high anisotropy, which makes it easy to cleave along the (100) plane compared to other planes. Fig. 14(a) shows the cleavage along the (100) plane on a (−201) substrate. The cleaved crystals can be further thinned down using the mechanical exfoliation technique using adhesive tape. Fig. 14(b) and (c) show optical microscopic images of the Ga_2O_3 membrane extracted from its substrate and the transferred membrane on top of the Si wafer. Standard device fabrication can be carried out on top of these membranes. Both depletion and enhancement mode devices were fabricated on Ga_2O_3 membranes with SiO_2 as the bottom gate.[81,82] These devices show the highest current densities among Ga_2O_3 devices.[82] As described above, the anisotropy of the Ga_2O_3 crystal can be exploited to fabricate large area crystalline membranes which can be transferred to high thermal conductivity substrates. This method could potentially overcome the low thermal conductivity challenge of Ga_2O_3 for power devices.

(5) Diamond membranes

Diamond is another attractive ultra WBG material that has superior electrical and mechanical properties such as high carrier mobility (*e.g.* hole mobility: ~1800 cm^2 V^{-1} s^{-1}), high saturation velocity (~3 × 10^7 cm s^{-1}), high thermal conductivity (up to 150 W cm^{-1} K^{-1}), a large band-gap (5.47 eV), and very high breakdown electric field (~10^7 V cm^{-1}).[83–85] To date, CVD has

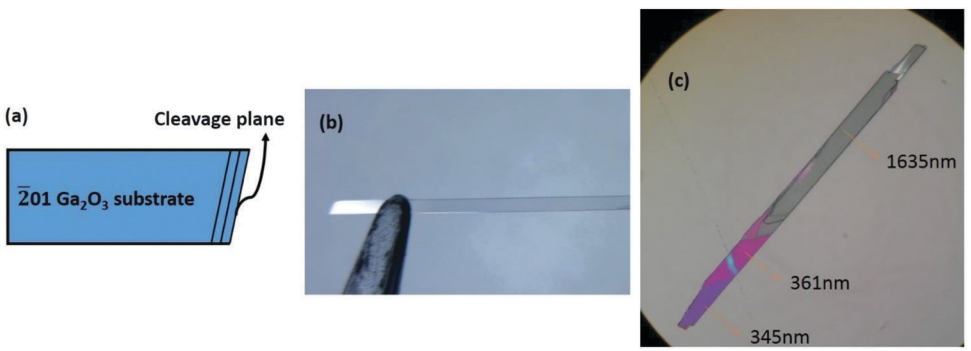

Fig. 14 (a) Cross-section schematic showing the cleavage plane in the Ga_2O_3 substrate. (b) Optical microscope images of the Ga_2O_3 membrane extracted from the Ga_2O_3 substrate. (c) Ga_2O_3 membrane transferred onto a Si wafer with the measured thickness of the membrane.

been the most popular method to grow homogenous single crystalline diamond on top of a single crystalline diamond plate.[86] In particular, advanced CVD systems such as filament-assisted thermal CVD, electron-assisted thermal CVD, laser-assisted thermal CVD, RF-plasma CVD, microwave-plasma CVD, combustion flame-assisted CVD, and direct-current arc plasma jet CVD were employed to grow a high-quality homogenous layer.[86–89] However, it is not possible to create free-standing diamond due to the absence of the lattice-matched sacrificial single crystalline layer. Instead, several approaches have been reported to create free-standing single crystalline diamond membranes. The first approach that was proposed by N. R. Parikh *et al.* employed high energy and high dose ion implantation to selectively damage a sub-surface of the diamond, followed by a lift-off process.[90] P. Olivero *et al.* further utilized the ion implantation method by employing focused ion beam (FIB) milling to vertically cut-out and create patterned diamond membranes.[91] Recently, J. S. Hodeges *et al.* reported the creation of high aspect ratio single crystalline diamond nanoslabs that were formed by deep etching. In the following section, we will review the details of the creation of single crystalline diamond membranes and their material characteristics, applications, and limitations.[92]

The high dose and high energy ion implantation method depicted in Fig. 15(a) by N. R. Parikh *et al.* has been widely used by others because this method offers precise control over the thickness of the diamond membranes.[90] This method uses a high dose (typically 10^{16} cm^{-2} or greater) and MeV range energy with helium, oxygen, or carbon ions to selectively damage a portion of the diamond, followed by thermal annealing at about 900 °C under vacuum to graphitize the damaged region. The implanted diamond sample is ready to separate either by

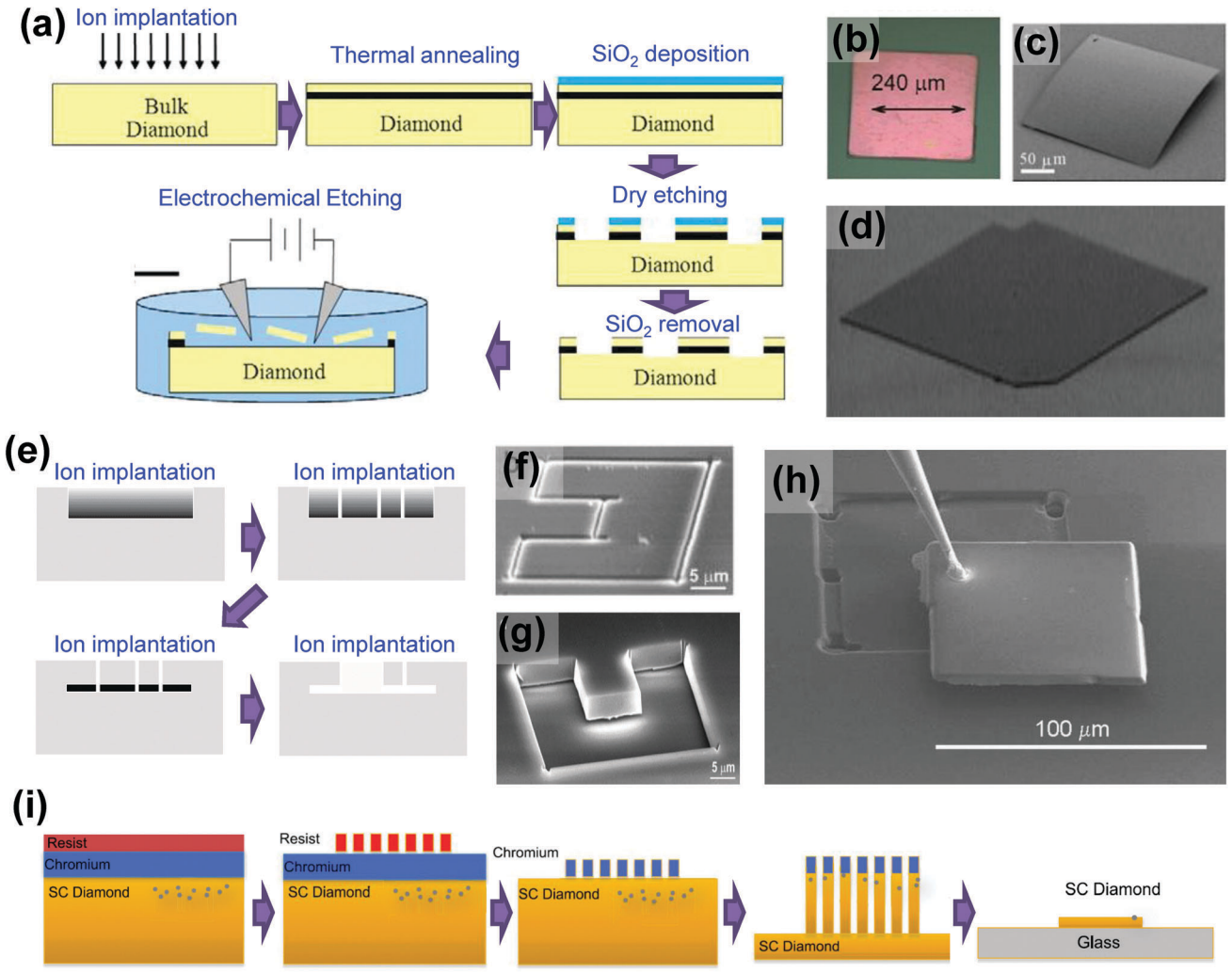

Fig. 15 (a) Schematic illustration of the procedure used to generate diamond membranes. (b) Microscopic image of the released single crystalline diamond membrane. (c) Single crystalline diamond membrane exhibiting curvature due to built-in strain. (d) A stamped and thinned membrane exhibiting uniform thickness without noticeable curvature. (e) Schematic diagrams illustrating the FIB-assisted lift-off process. (f and g) SEM images of the FIB patterned area. (h) The SEM image shows the freshly exposed layer as the cap is lifted away after being attached to the probe with platinum. (i) Fabrication of nanoslabs in ultra-pure diamond. Reproduced with permission from ref. 89, 91 and 92. Copyright 1992, 2012, and 2013, American Institute of Physics, IOPscience, and Elsevier.

immersing it in chromic-sulfuric acid or by electrochemical etching. The major drawback of this approach is that ion implantation induces a built-in strain and degrades the optical properties in the diamond membrane as a result of the high ion damage and following the high-temperature annealing process (Fig. 15(b) and (c)). J. C. Lee *et al.* improved these issues by a short overgrowth of diamond on a bulk diamond template.[93] The thinnest single crystalline diamond membrane formed using the ion implantation method is 190 nm. P. Olivero *et al.* used FIB milling to create a patterned diamond membrane as shown in Fig. 15(e)–(h).[92] This method not only allows us to form various suspended diamond membrane structures, but also gives us more freedom to make different shapes of diamond membranes which are not possible using the earlier methods.

J. S. Hodeges *et al.* took a different route to create a single crystalline diamond membrane.[93] As described in Fig. 15(i), the fabrication began with line patterning on a single crystalline diamond plate, followed by deep etching using an inductively coupled plasma (ICP) etcher with O_2 gas. Because the length of the patterns and the depth of diamond will be the length and the width of the diamond membrane after the completion of the process, this approach offers some freedom in changing the dimensions of the diamond membrane. Once the deep etching step is completed, each slab can be exfoliated from the diamond substrate and precisely positioned on a foreign substrate using a PDMS transfer method. This approach has a clear advantage over the ion implantation method because it does not produce any built-in strain or degradation in the optical properties. However, this method still needs to be polished to overcome scalability and surface roughness issues that are mainly associated with the etching process such as different plasma density during etching, relatively slow etching rate, and non-perpendicular side wall angle.

To date, the most popular applications using single crystalline diamond membranes have been photonic devices due to the presence of nitrogen-vacancy (NV) centers in diamond.[94,95] The NV centers in diamond allow us to utilize diamond as a unique platform for a quantum information processing device because it offers superior optical addressability and readout, high-fidelity state preparation, and long spin coherence time with a controllable set of ancilla qubits at room temperature.

As shown in Fig. 16(a), P. Olivero *et al.* first demonstrated a single crystalline diamond waveguide by forming a 2 μm × 60 μm free-standing waveguide using the FIB lift-off method and achieved multimode light propagation which is estimated to be more than 10 propagation modes using a 532 nm laser source.[91] A. D. Greentree *et al.* utilized the method by nitrogen implantation and demonstrated single spin read-out and qubit control which showed the potential of the single crystalline diamond membrane as a material for quantum computing devices (Fig. 16(b)).[96] Other photonic devices such as high-quality factor micro-ring cavities (Fig. 16(c) and (d)) or cantilevers (Fig. 16(e)) that have a vibration frequency up to 1 MHz were reported using the same FIB lift-off method.[97] As shown

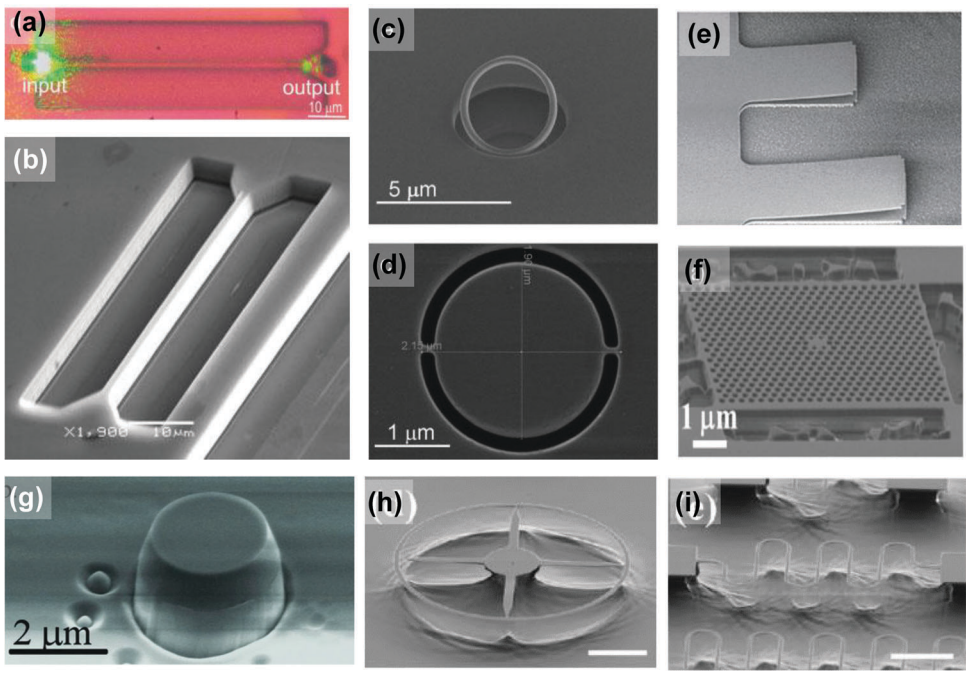

Fig. 16 (a) Coupled through the single crystalline diamond membrane bridge structure. (b) SEM image of a waveguide structure created in single crystalline diamond with the FIB assisted lift-off technique. (c) Micrometer-scale ring, a prototype for a whispering gallery mode resonator, fabricated in a 330 nm layer of single-crystal diamond. (d) Concept cavity with 1.9 mm inner diameter and 2.2 mm outer diameter. (e) Single crystalline diamond cantilevers with lengths of 50 and 70 μm and a width of 40 μm. (f) SEM image of the diamond membrane photonic crystal cavities. (g) A typical SEM image of a microdisk cavity with a diameter of 2.5 mm and a thickness of ~800 nm. (h) ~500 nm wide nanoring structure. (i) ~500 nm wide curved nanobeams. Reproduced with permission from ref. 90, 92 and 95–98. Copyright 2005, 2013, 2006, 2008, and 2012, Wiley-VCH, Elsevier, IOPscience, American Chemical Society.

in Fig. 16(f), J. Lee *et al.* used ion-implantation to fabricate diamond photonic crystals and reported a cavity mode with a quality factor of 1000.[93] Resonators that can operate up to 25 MHz were realized by I. Aharonovich *et al.* using ion implantation followed by diamond re-growth (Fig. 16(g)).[98] The various nanophotonic structures (Fig. 16(h) and (i)) demonstrated by M. J. Burek *et al.* using angled plasma etching promise great potential toward free-standing diamond photonic applications.[99]

Compared with device applications using other free-standing WBG materials, the development of free-standing diamond membrane-based devices is far behind, primarily because of the intricate membrane fabrication process. Recent progress in diamond processing toward a lower temperature process such as low-temperature selective doping will contribute to lowering the technical barrier.[100] Nonetheless, free-standing single crystalline diamond membranes have myriad potential toward future power electronics, implantable electronics, and optoelectronics that can form either a heterostructure with other semiconductors or non-rigid geometry toward flexible devices due to its high electric-field handling capability, superior bio-comparability with good corrosive resistance as well as the widest transmission spectrum covering from UV to the microwave range, while maintaining nanometer thinness.

3. Conclusion

In summary, we have presented recent advances in free-standing WBG semiconductor membranes. By introducing lift-off techniques, WBG membranes are delaminated from their bulk substrates, allowing them to be transferred onto arbitrary substrates. The material investigations (*e.g.*, XRD, PL, Raman, and TEM, *etc.*) show that the material qualities of WBG membranes are comparable to those of their bulk counterparts. This enables WBG membranes to be one of the ideal candidates for unique applications such as flexible high performance electronic and optoelectronic devices. Detailed examples include flexible GaN LEDs and UV ZnO PDs. In addition, it will be possible that WBG membranes will be the building blocks for vertically stacked heterojunction devices if an electrically stable interface is obtained. It is promising that this material platform will bring versatile applications which their bulk materials cannot realize.

Acknowledgements

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